

**Remarks**

This is responsive to the Office Action mailed September 12, 2007. Claims 1-18 and 21-25 are pending. Claims 6-14 are allowed. Claims 1-5 and 15-25 are rejected. Claims 16 and 21 have been amended. Claims 19 and 20 have been canceled.

Applicant thanks the Examiner for the teleconference of November 19, 2007, and hopes that in light of the interview, this paper will place all pending claims in condition for allowance.

**Drawing Rejections**

The Examiner objects to the drawings as failing to comply with 37 CFR 1.84 (p)(5) because item 350 shown in Figure 3 is not referenced in the specification. Corrected Figure 3 is submitted herewith. Applicant has removed the reference numeral “350” from the drawing.

**Rejection Under 35 U.S.C. §112**

Claims 1-5, 15-18, and 21-25 stand rejected under 35 U.S.C. §112 as failing to comply with the enablement requirement. This rejection is respectfully traversed.

Applicant appreciates the Examiner’s clear exposition of this rejection on page 5 of the Official Action of 9/12/2007. However, Applicant believes that the Examiner has made the claims appear to be unclear by reading limitations and conditions into the claims that do not appear there, even when considered in light of the specification.

The Examiner has characterized the interface 450 in the specification as “bi-directional communications links.” The Examiner then equates his own characterization

of the interface 450 to a number of buses. Applicant does not necessarily agree with this characterization. However, assuming for the sake of argument that the Examiner's characterization is correct, the use of a single bus as it is used in the claims is nevertheless enabled under 35 U.S.C. §112 because each of the rejected claims is written in open or "comprising" form. This means that the apparatus and methods of the claims are not strictly limited to those steps or structures recited. It goes without saying that any infringing device (and any anticipating reference) would, however, have *at least* those elements recited.

Referring to independent claim 1, the preamble of the claim states "In an apparatus having *a bus* operatively coupled to a first controller chip and a first channel chip... the apparatus also having a storage medium operatively coupled to *the bus* through a storage medium interface." The claim elements then recite "retrieving a first portion of the recorded data via *the bus*," "updating some of the registers via *the bus*," and "retrieving a second portion of the recorded data via *the bus*." Therefore, this claim will be enabled according to 35 U.S.C. §112, 1<sup>st</sup> paragraph, if it can be shown in the specification that a single bus is adequately described as fulfilling all these functions, regardless of any other buses or structures that may appear in the specification. Clearly, the exemplary bus that meets this requirement is the bus 360, described repeatedly in the specification as being used for both updating registers and transferring data.

Independent claim 15 requires "*a bus* operatively coupled between the interface and the chips, *the bus* controllable by the DMS controller to read from the memory and to update several of the registers in response to a zone transition event." As long as a single

bus may be found in the specification that satisfies this claim language, this claim is in compliance with 35 U.S.C. §112. Clearly this is the bus 360.

The situation is the same with independent claims 16 and 21. Claim 16, as amended for reasons unrelated to this rejection requires, “providing data from a storage medium via *a bus*, *the bus* operatively connected to at least one register, the storage medium, and a controller chip … updating the at least one register or parameter via *the bus* … and… providing data from the storage medium via *the bus* responsive to the updating.” Claim 21, as also amended for separate reasons, requires “A method for reducing processing burden on a processing device, comprising steps of transmitting first data from a storage medium via *a bus* coupled to the processing device, updating at least one register or parameter via *the bus*, and transmitting second data from the storage medium via *the bus* in response to the updating step.” Once again, for both of these claims, bus 360 is described in the specification as fulfilling the claimed role and therefore the claims are in compliance with 35 U.S.C. §112. This is true regardless of what other buses or components may appear in the specification since the claims are in open or “comprising” form, rather than a closed form.

In addition to the foregoing, the limitations to which the Examiner is now objecting in the current claims appeared in a similar form in the originally filed claims. See, for example, originally filed claim 1:

In a storage system having *a bus* operatively coupled to a first channel chip, the channel chip having several registers, the storage system also having a storage medium operatively coupled to *the bus* through a storage medium interface, a method for retrieving data recorded on a storage medium comprising the step of:

- (a) retrieving a first portion of the recorded data via *the bus*;
- (b) updating some of the registers via *the bus*; and
- (c) retrieving a second portion of the recorded data via *the bus*.

It is a settled point of law that originally filed claims are a part of the specification. For example, *In Re Gardner* states “Under these circumstances, we consider the original claim in itself adequate ‘written description’ of the claimed invention. It was equally a ‘written description’ whether located among the original claims or in the descriptive part of the specification,” 178 USPQ 149, 149 (C.C.P.A. 1973). Therefore, there is an additional and adequate basis for withdrawal of the 35 U.S.C. §112 rejection, which is respectfully requested.

Dependent claims 4-5, 17-18, and 22-25 are rejected based upon their dependency to the independent claims rejected above. Since the rejection of the corresponding independent claims has been addressed, withdrawal of the rejection of the remaining dependent claims is also requested.

#### **Rejection of Claims Under 35 U.S.C. §102**

Claims 1-3, 5, 16, and 18 stand rejected as being anticipated by U.S. Patent No. 5,276,564 to Hessing ('564). This rejection is again respectfully traversed. Applicant has previously argued before the Examiner the points made below. Applicant respectfully requests that the Examiner reconsider them now in view of the recent interview.

Hessing '564 discloses transferring recorded data from read channel 12 to data path controller 26 via a serial data bus formed by decoded serial read data path 36 and read clock path 38. (Hessing '564, col. 3 lines 25-27). Hessing '564 further discloses using a separate system bus 50 to pass data from ROM 23 to timing generator 20 to update registers 74, 76. (Hessing '564, col. 5 lines 24-26) The serial data bus and the

system bus in Hessing ‘564 are different and separate data paths rather than the single bus required in the independent claims of the Applicant.

To interpret Hessing ‘564 otherwise leads to the conclusion that two discrete and unconnected buses connecting different sets of components are part of the same bus. That is, that the serial data bus (connecting the read channel 12 and the controller 26) and the system bus (connecting the servo timing generator 20 and the controller 26) form a single bus. Clearly this interpretation is not supported. This is recognized by the Examiner’s own 35 U.S.C. §112 rejections of the Applicant’s claims for identifying multiple buses in the specification but only a single bus in the claims.

The Microsoft Computer Dictionary, cited previously by the Examiner as extrinsic evidence defines a bus as “a set of hardware lines used for data transfer among components of a computer system....” Thus a first set of hardware lines connecting two or more components is a separate bus from a second set of hardware lines connecting two or more components.

Referring now to independent claim 1, the preamble of the claim states “In an apparatus having *a bus* operatively coupled to a first controller chip and a first channel chip... the apparatus also having a storage medium operatively coupled to *the bus* through a storage medium interface.” The claim elements then recite “retrieving a first portion of the recorded data via *the bus*,” “updating some of the registers via *the bus*,” and “retrieving a second portion of the recorded data via *the bus*.” Because Hessing ‘564 contemplates a plurality of buses to obtain these functions, Hessing ‘564 fails to teach each and every element of claim 1, wherein *a single bus* is claimed.

Amended claim 16 similarly requires, “A method comprising steps of: (a) providing data from a storage medium via *a bus*, *the bus* operatively connected to at least one register, the storage medium, and a controller chip; (b) updating the at least one register or parameter via *the bus*; and (c) providing data from the storage medium via *the bus* responsive to the updating..” Again, Hessing ‘564 fails to teach every element of claim 16 because Hessing ‘564 contemplates a plurality of busses to obtain these functions.

Claims 2-5 depend from and further limit claim 1 and claims 17 and 18 depend from and further limit claim 16. Therefore these claims should also be allowable over Hessing ‘564 or combinations requiring Hessing ‘564.

Claims 16, 18, and 21 stand rejected as being anticipated by U.S. Patent No. 6,260,095 to Goodrum.

Claim 16 has been amended and now recites “A method comprising steps of: (a) providing data from a storage medium via a bus, the bus operatively connected to at least one register, the storage medium, and a controller chip; (b) updating the at least one register or parameter via the bus; and (c) providing data from the storage medium via the bus responsive to the updating.”

Applicant submits that Goodrum ‘095 does not teach or submit a bus connected to a storage medium, a register, and a controller chip that is operable in the manner claimed. As discussed above, Applicant also believes that Hessing ‘564 fails to teach or suggest the claimed subject matter. Applicant therefore submits that claim 16 and claim 18, which depends from and further limits claim 16, should be allowable over the art of record.

Claim 21 has been amended to recite “A method for reducing processing burden on a processing device, comprising steps of transmitting first data from a storage medium via a bus coupled to the processing device, updating at least one register or parameter via the bus, and transmitting second data from the storage medium via the bus in response to the updating step.” Applicant contends here also that neither Goodrum ‘095, nor Hessing ‘564, teaches a bus coupled to a processing device, a storage medium, and a register that is capable of performing as claimed. For this reason, at least, claim 21 should be allowable over the art of record.

**Rejection of Claims Under 35 U.S.C. §103(a)**

Independent claim 15 stands rejected as being unpatentable over Hessing ‘564 in view of Taniai ‘665. Applicant traverses this rejection on the grounds that the Examiner has not borne his burden of establishing a *prima facie* case of obviousness because the cited references do not combine to teach every element of claim 15.

Claim 15 recites in part “a bus operatively coupled between the interface and the chips, the bus controllable by the DMA controller to read from the memory and to update several of the registers in response to a zone transition event.” The Examiner has relied on Hessing ‘564 to satisfy this claim element based on the assertion that all signal lines of Hessing ‘564 are regarded as the same bus. Applicant has addressed this interpretation of Hessing ‘564 regarding claims 1-3, 5, 16, and 18 above. Here again, Applicant submits that Hessing ‘564 does not teach or suggest the bus of the Applicant’s claims. For this reason, at least, claim 15 should be allowable over the combination of Hessing ‘564 and Taniai ‘665.

**Allowable Subject Matter**

The Applicant gratefully acknowledges the allowance of claims 6-14.

**Conclusion**

This is believed to be a complete response to the Office Action of September 12, 2007. Reconsideration and allowance of all pending claims is respectfully requested. Should the Examiner have any questions regarding this response, or can see any reason that the remaining claims should not be allowed, he is invited to telephone the undersigned attorney.

Respectfully submitted,

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